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*Please replace the paragraph on page 3, lines 1-13, with the following:*

Q<sup>2</sup>

In one embodiment of the invention, a system and methods are provided for interfacing a computer system or other network entity to an Ethernet network, and for transferring data to and from the entity at multiple gigabits per second.

*Please replace the paragraph on page 4, lines 10-17, with the following:*

Q<sup>3</sup>

Illustratively, the size of each mini-frame of an Ethernet frame (i.e., the portion of the frame carried by one channel) will equal the size of the other mini-frames, plus or minus one byte. This provides one easy method of detecting an error in the transmission or reception of a frame. Further, frame sequencing may be enforced by providing multiple different codes or symbols to represent the period between frames (e.g., the Inter-Packet Gap or IPG). With this method of frame sequencing, a receiving entity may synchronize the multiple channels by monitoring which codes or symbols are received during each gap.

*Please replace the paragraph on page 6, lines 21-25, with the following:*

Q<sup>4</sup>

In one embodiment of the invention, an interface is described for connecting a computer system to an Ethernet network at a data transfer rate exceeding 1 Gbps. In one particular implementation of this embodiment, the network interface exchanges communications with the Ethernet network at a rate of approximately 10 Gbps.

*Please replace the paragraph on page 9, lines 14-24, with the following:*

Q<sup>5</sup>

In the illustrated embodiment, the design and operation of 10GMII 102 and each 2GMII 104 are based on the full duplex subset of the GMII described in the IEEE 802.3 standard. During operation of the embodiment depicted in FIG. 1, distributor/collector 100 receives frames, or packets, from a Medium Access Control (MAC) layer through 10GMII 102 at a rate in excess of 1 Gbps (e.g., up to approximately 10 Gbps in the illustrated embodiment). Similarly, distributor/collector 100 operates in the reverse direction to provide a MAC layer with reconstructed frames at the same rate of transfer. This transmission rate is approximately equal to the sum of the rates at which data are transferred across the 2GMII interfaces that connect distributor/collector 100 to each PCS. Thus, in FIG. 1, each 2GMII may operate at a rate of approximately 2.5 Gbps.